Faculty and Research Interests

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Education:

- Ph.D. in CS, National Tsing Hua University, 2006
- M.S. in CS, National Tsing Hua University, 2000
- B.S. in PHYS, National Tsing Hua University, 1997

Experience:

- 2017 – now Associate Professor, CSIE, NTUST
- 2014 – 2017 Associate Professor, CSE, YZU
- 2006 – 2014 Associate Professor, CSE, YZU

Recent Research Interests:

- Electronic Design Automation/Computer Aided Design
- Multicore Computer Architecture
- FPGA and Embedded System Design

CAD Lab Honors :

- Excellent Presentation Award, IPS, 2006.
- CAD Contest Third Place, 2009, 2010, 2012.
- ACM-ICPC NCPU First Place, 2011, 2012.
- Teaching Excellence Award, YZU, 2014.

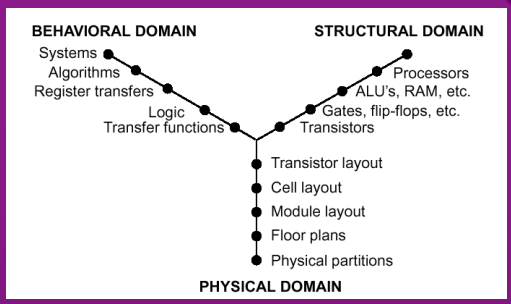
Recent Projects:

[Ministry of Science and Technology]

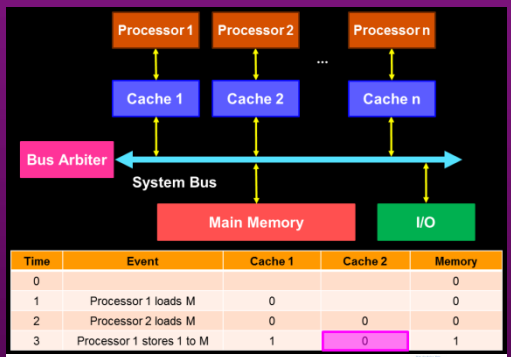
- GPU Accelerated Computing Framework for EDA
- Dual-addressing Memory Design and Optimization
- Power Integrity Enhancement Methodology

[Ministry of Education]

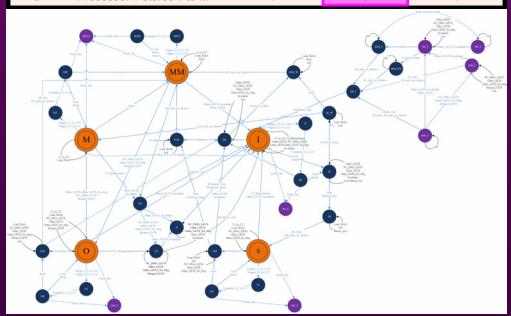
- Course Development for Cache Organization
- Course Development for Cache Coherence
- Course Development for Advanced Cache Topics
- Course Development for Computer Organization



EDA enables IC design, verification, synthesis, floorplan, placement, route, design rule check, etc. via efficient *CAD* algorithms.



Time	Event	Cache 1	Cache 2	Memory
0				0
1	Processor 1 loads M	0		0
2	Processor 2 loads M	0	0	0
3	Processor 1 stores 1 to M	1	0	1



Cache coherence intends to keep shared cache data consistent in a multicore system when there are more than one processing units sharing the same memory data.